REMARKS

This response amends claims 1-4, 14, 34, 38-39 (mostly for clarifying the claim language), cancels claims 8-10, 13, 31, 35 and 37, and adds new claims 40-74. Support for the amendments and claims can be found, e.g., at pages 6-12 of the specification. Upon amendment, this application will have 11 independent claims (claims 1, 2, 34, 38, 39, 52, 53, 60, 61, 65 and 69) and 44 total claims (claims 1-5, 14, 34 and 38-74). Enclosed please find a form and fee for excess claims.

In section 1 of the Office Action, the Examiner objects to claims 1-4, 8-10, 13-14, 31 and 39, asserting that it is unclear whether the term "comprising" in claims 1, 2, 31, and 39 refers to the first circuit, the second circuit, or both circuits. The objected word "comprising" has been amended to "the second circuit comprising". The Applicants believe that this objection has been overcome.

In section 2, the Examiner objects to claims 8-9, asserting that it is unclear whether the doped region recited in claim 1 is the same element as the fourth doped region recited in dependent claim 8. The term "doped region" in claim 1 has been amended to "the fourth doped region". The Applicants believe that claims 8-9 are now clear and the objection in this regard has been overcome.

In sections 3-6 of the Office Action, the Examiner rejects claims 34, 35, 37 and 39 under 35 USC 112, first paragraph, asserting that there is no

support in the specification for a device which comprises no DC connection to the first node, no DC connection between the first doped region and the pad, and a first doped region capacitively coupled to the pad.

As shown in Fig. 2, a DC connection V_{DD} is coupled to the first node and the pad. However, in the present invention, if the DC power V_{DD} is coupled to the pad (or node), the DC power V_{DD} is then coupled to the region 24 through the N well region 18 and the region 22. At the same time, the DC power V_{DD} is not coupled to third doped region 30 because of a PN junction (depletion capacitor) between the region 30 and the well region 18. Thus, support for claims 34 and 39 can be found in figures and specification of the present invention.

In sections 6-9 of the Office Action, the Examiner asserts that there is no support in the specification for a device which comprises a first doped region capacitively coupled to the pad and electrically floated in the well and has no DC connection between the first doped region and the pad as cited in claim 39 respectively. Typically, a capacitor is used to isolate DC component of signals. Thus, the DC power VDD is not coupled to third doped region 30 because of a depletion capacitor (PN junction) between the region 30 and the well region 18. Similarly, even if a capacitor is coupled between the first doped region and the pad, the DC power VDD is also not coupled to the first doped region 30 when the DC power VDD is coupled to the pad. Thus, support for claim 39 can be found in figures and specification of the present invention.

In section 10 of the Office Action, the Examiner asserts that claim 39 is unclear as to what is meant by a DC connection between two elements, since DC connection is the coupling of an element of a power source. The first node or the pad are used to convey signals (DC signals, AC signals, Power sources, or any signals) to the internal circuit, and the region 20 of the output buffer (or ESD protection circuit) of the present invention is also coupled to the pad or the first node (when the transistor P1 is turned on). Thus, a DC connection between the elements is the same as the coupling of an element to a power source.

Rejections under 35 USC 102(b)

In section 12, claims 34-35 and 37 are rejected under 35 USC 102(b) as being anticipated by Ham (US Patent No. 5,903,420) or Avery (US Patent No. 5,343,053). In section 12, claim 38 is rejected under 35 USC 102(b) as being anticipated by Wu (US Patent No. 5,686,751). These rejections are respectfully traversed.

Ham discloses an ESD protecting circuit for effectively discharging an overcurrent by providing a plurality of current paths. In Ham, if the first conductive type of the substrate 20 is N type and the first conductive type of the doped region 46 is N type, the region 46 of N type is electrically coupled to the V_{DD} through the N-well 24 and the region of N type 52. Alternately, as the first conductive type of the substrate 20 is P type in Ham, the first conductive type of the doped region 46 is P type also. At this time, the region 46 is electrically coupled to the V_{SS} through the P-well 22

and the region of P type 40. Thus, the doped region 46 in Ham is not electrically floated whether the conductivity type thereof is an N type or P type. **Furthermore, in amended claim 34, the third doped region is disposed within the well region. However, the doped region 46 in Ham is not within the well region (22 or 24), and the doped region 46 is extending outside the well region (22 or 24).** Thus, the 102 rejection of claim 34 by Ham is respectfully traversed, as Ham does not teach, disclose or suggest an electrically floated doped region recited in claim 34.

Avery teaches an ESD protection circuit having a zener diode in parallel therewith for turning on the SCR, and a zener diode in series therewith to control the "on state" or clamping voltage, as cited in column 2, lines 3-8. Thus, all P type doped regions (36, 136, 236, 336, 436, 56 and 156) in the N-well regions (34, 134, 234, 334, 434, 54 and 154) as shown in Figs. 4~11 make contact with the pad-connected N doped region to form a needed zener diode in series with the SCR 112. For example, the P type doped region 36 makes contact with third region 40 coupled to the pad 47 to form the zener diode 114, in series with the SCR 112, as recited in column 3, lines 52~58. Thus, Avery teaches the P type floating region (36, 136, 236, 336, 436, 56 and 156) making contact with a pad-connected N doped region to form a zener diode. However, **in the amended claim 34, the third doped region 30 is disposed in the well region 18, and is spaced apart from the fourth doped region 20, which is coupled to the pad.** Avery **teaches away** from the floating region as claimed in claim 34, and does not teach all features in claim 34. Thus, the 102 rejection of claim 34 is respectfully traversed.

In section 13 of the Office Action, the Examiner asserts that Wu teaches all features as recited in claim 38. In the present invention, the first doped region 24 as claimed in claim 38 is coupled to the first node (pad) through the fourth doped region 20, the well region 20 and the fifth doped region 22. The third doped region 30 is coupled to the first node (pad) through a capacitor Cn.

However, the doped regions of the second conductivity type in the well region 220 in Wu are regions 225, and thus the two regions 225 correspond to the first dope region and the second doped region as the Examiner asserts that a second doped region 225 is a second conductivity type, formed in the first conductivity substrate. Further, Wu teaches the contact regions 225 of P+ type being connected to the VSS (second node) because the contact regions 225 are bulk terminal of the second MOS transistor M7 as recited in column 6, lines 29-31. Further, layer 232 is a pad as recited in column 6, line 56. As shown in Fig. 6, because the Examiner asserts that the second region 225 is connected to a second node (VSS), **there is no first doped region coupled to a first node when both regions 225 are coupled to together to second node VSS.** Accordingly, in Wu, there is no first doped region coupled to the pad 232 through the fourth doped region 20, the capacitor Cn and the fifth doped region 22, wherein the fourth and the fifth doped region (22 and 23) are the second conductivity type. Thus, Wu does not teach all limitation as claimed in claim 38. Therefore, the 102 rejection of claim 38 by Wu is respectfully traversed.

Rejections under 35 USC 103(a)

In section 15, claims 1, 3-4, 8, 13-14, 31, 34-35, 37 and 39 are rejected under 35 USC 103(a) as being unpatentable over Ham in view of Applicant's Admitted Prior Art (AAPA). In section 16, claims 1, 8-9, 13-14, 31, 34-35, 37 and 39 are rejected under 35 USC 103(a) as being unpatentable over Avery in view of AAPA. In section 17, claim 2 is rejected under 35 USC 103(a) as being unpatentable over Wu in view of AAPA. These rejections are respectfully traversed.

The combination of Ham and AAPA

In section 15 of the Office Action, the Examiner asserts that Ham teaches substantially the entire claimed structure in claims 1, 34 and 39 unless first and second circuit coupled between first and second power lines and a pad. The Applicants respectfully disagree.

In Ham, if the first conductive type of the substrate 20 is N type and the first conductive type of the doped region 46 is N type, the region 46 of N type is electrically coupled to the V_{DD} through the N-well 24 and the region of N type 52. Alternately, as the first conductive type of the substrate 20 is P type in Ham, the first conductive type of the doped region 46 is P type. At this time, the region 46 is electrically coupled to the VSS through the P-well 22 and the region of P type 40. Thus, the doped region 46 in Ham is not electrically floated whether the conductivity type thereof is an N type or P type. **Furthermore, the doped region 46 in Ham is not within the well region (22 or 24), and the doped region 46 is xt nding**

outside the well region (22 or 24). In amended claim 34, however, the third doped region is disposed within the well region. Thus, the 103 rejection of claim 34 by Ham in view of AAPA is improper, as neither Ham nor AAPA teaches, discloses or suggests an electrically floated doped region recited in claims 1, 34 and 39. Insofar as claims 3-4, 13-14 depend from claim 1, it is the Applicants' belief that these claims are also patentable.

The combination of Avery and AAPA

Claims 1, 13-14, 34 and 39 are rejected to under U.S.C 103(a) as being unpatentable over Avery (5343053) in view of AAPA. These rejections are respectfully traversed.

Avery teaches an ESD protection circuit having a zener diode in parallel therewith for turning on the SCR, and a zener diode in series therewith to control the "on state" or clampling voltage, as cited in column 2, lines 3-8. thus, all P type doped regions (36, 136, 236, 336, 436, 56 and 156) in the N-well regions (34, 134, 234, 334, 434, 54 and 154) as shown in Figs. 4~11 make contact with a pad-connected N doped region to form a needed zener diode in series with the SCR 112. For example, the P type doped region 36 makes contact with third region 40 to form the zener diode 114 in series with the SCR 112, as recited in column 3, lines 52~58. Thus, Avery teaches the P type floating region (36, 136, 236, 336, 436, 56 and 156) contacting with a pad-connected N doped region to form a zener diode. **However, in the amended claims 1, 34 and 39, the third dop d region 30 is disposed in the well region 18, and is space apart from the fourth**

doped r gion 20 that is coupl d to the pad. Thus, Avery teaches away from the floated region as claimed in claims 1, 34 and 39. Claims 1, 34 and 39 should be patentable because neither Avery nor AAPA teaches a floating doped region 30 as claimed. Insofar as claims 3-4, 13-14 depend from claim 1, it is the Applicants' belief that these claims are also patentable.

The combination of Wu and AAPA

Claim 2 is rejected to under U.S.C 103(a) as being unpatentable over Wu (5686751) in view of AAPA. In section 17 of the Office Action, the Examiner asserts that Wu teaches all features as recited in claim 2 except that first and second circuits are coupled between first and second power lines and a pad. The Applicants respectfully disagree.

In claim 2, the resistor has a first end 20 coupled to a pad and a second end 22 coupled to the ESD protection component. In Wu, the doped regions of the second conductivity type in the well region 220 are regions 225, and thus the two regions 225 correspond to the first end and the second end as claimed in claim 2 as the Examiner assert that the resister constructed by well region 220 has a first end (region 225) coupled to VSS. However, the contact regions 225 of P+ type being connected to the VSS (second node) because the contact regions 225 are bulk terminal of the second MOS transistor M7 as recited in column 6, lines 29-31. **As taught by Wu, the pad is connected to the VSS if the first end (region 20) and the second end (region 22) are both coupl d to th VSS (second node) at the sam time. At this tim , th output buffer**

claimed in claim 2 cannot work, and thus, Wu teaches away from output buffer as claimed, and there is no resistor constructed by a well region in Wu. Further, the regions 225 (first end) are not coupled to the pad in Wu. Neither Wu nor AAPA teaches a resistor with two ends of the second conductivity type as claimed. Thus, the Applicants believe that the 103 rejection of claim 2 should be withdrawn.

Due to the reasons stated above, the Applicants respectfully submit that all pending claims are patentable and reconsideration of this application is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

Enclosed please find a copy of Troy Guangyu Cai's Notice of Limited Recognition under 35 CFR 10.9(b) to prepare and prosecute patent applications wherein the patent applicant is a client of Ladas & Parry, and the attorney of record in the applications is a registered practitioner who is a member of Ladas & Parry.

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(Date of Deposit)

Troy Guangyu Cai
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